Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants disclosed and claimed invention.

Support for the amendments is found in the original claims and the Specification.

No new matter has been added.

For example support for the amended claims is found in the original claims and in the Specification in Figures 1D-1F and at paragraphs 0021 and 0022:

"Referring to Figure 1D, in an important aspect of the invention, sidewall spacer dielectric material, for example including one or more layers e.g., 26 of silicon oxide (SiO_2), silicon nitride (e.g., SiN), and silicon oxynitride (e.g., SiON) is deposited, for example using a blanket (e.g., substantially conformal) deposition process such as LPCVD, PECVD or HDP-CVD, to about a thickness of a desired sidewall spacer width, for example equal to or greater than the predetermined distance D to at least partially, **preferably**

substantially fill the space defined by distance D between pass transistor 22A and storage capacitor 22B. The thickness of the layer 26 for example, is between about 500 Angstroms and about 2000 Angstroms.

Referring to Figure 1E, a conventional wet or dry etchback process, preferably a dry (plasma enhanced) etchback process is then carried out to etchback sidewall spacer dielectric layer 26 to form sidewall spacers e.g., 26A and leaving a sidewall spacer layer portion 26B remaining between the storage capacitor 22B and the pass transistor 22A to cover P doped region 24B following the plasma enhanced etchback process. Advantageously, by forming pass transistor portion 22A and storage capacitor 22B to have a predetermined distance D between the respective structures of less than about twice a sidewall spacer width, the sidewall spacer etchback process leaves an unetched dielectric sidewall spacer layer portion e.g., 26B, covering the P-doped region 24B thereby forming an implant mask in a subsequent ion implant process e.g., HDD, to form a more heavily doped contact region e.g., 24A.

Claim Rejections under 35 USC 102(b)

Claims 1, 2, 5-9, 12, 13, and 16-19 stand rejected under 35 USC Section 102(b) as being anticipated by Leung et al. (US 6,468,855).

Leung et al. disclose a reduced topography DRAM cell that includes an access transistor and a storage capacitor (see

Abstract). In one embodiment, Leung et al. discloses a layout for the DRAM cell which "region 312 is laid out with minimum polysilicon gate spacing, which **is comparable to twice the size of the insulating sidewall spacers** 325". Leung et al. also disclose **forming sidewall spacers within the space between the pass transistor and the storage transistor** (see Figure 3E item 325 **overlying P- region,** item 312). Leung et al. do not disclose or teach a method for forming the sidewall spacers but do teach that "S/D doping and salicide are effectively excluded from region 312 without the need for additional processing steps." Leung et al. then teach carrying out an ion implanting process to form a **P doped region** (second doped region) (see Figure 3E, item 11; col 8, lines 57 to col 9, line 24).

Leung et al. does not disclose several aspects of Applicants disclosed and claimed invention including:

"depositing a spacer dielectric layer;

etching back the spacer dielectric layer to **form an ion implant mask fully covering** the first doped region while forming a sidewall spacer of a predetermined width overlying a first

portion of the second doped region; and,

carrying out a second ion implantation process to form a **P+** doped region in a second portion of the second doped region **while retaining the P- doped region** in the first doped region."

Thus, Leung et al. is insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Since Leung et al. fails to anticipate Applicants disclosed and claimed invention with respect to Applicants independent claims, neither does Leung et al. anticipate Applicants dependent

claims.

Claim Rejections under 35 USC 103(a)

1. Claims 10 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., above.

Applicants reiterate the comments made above with respect to Leung et al.

Leung et al. teach forming sidewall spacers within the space between pass transistor and the storage capacitor structure and do not teach or disclose a method for forming the sidewall spacers or teach forming an ion implant mask fully covering the first doped region.

As noted by Examiner, Leung et al. also do not teach forming a **P+ doped region in a second portion of the second doped region while retaining the P- doped region in the first doped region.**

Examiner refers to a second embodiment shown in Leung et al. (Figures 4A-4V) which shows a completely different device and

method for forming the same i.e., a complicated process for forming a **non-planar capacitor structure** where the non-planar capacitor is formed **partially on** the **P- doped region** (first doped region) (see e.g., Figure 4I, item 44), i.e., the non-planar capacitor structure is formed **following formation** of the P- region (see e.g., Figure 4A). **A P+ doped region** (second doped regions) is then formed by ion implantation while **masking a small portion of the P- region not already covered by the non-planar capacitor structure.** Figures 4K - 4V show another non-planar capacitor structure where the first and second regions are formed as **P+ regions** (see e.g., items 417 and 418, Figure 4R), where the **first doped P+ region contacts another P- region underlying apportion of the non-planar capacitor structure.**

The additional embodiments having non-planar capacitor structures have a significantly different structure and operate by a **different principle of operation** than the planar capacitor structure of Leung et al. shown in Figure 3E.

Thus there is no motive to combine the different embodiments as Examiner has attempted to do. There is no suggestion that the first and second doped regions in the planar capacitor structure

of Leung et al. should be or could successfully be formed as respectively, P+ and P- doped regions. Moreover, the method of formation as disclosed in the non-planar capacitor embodiments **(where the capacitor structure is formed following formation of the first doped region and partially overlying the first doped region)** could not successfully produce the planar capacitor embodiment of Leung et al., or Applicants disclosed and claimed invention. IN addition, any modification of the non-planar capacitor embodiments (methods and structures) in an effort to reproduce Applicants disclosed and claimed invention would make the non-planar capacitor methods and structures of Leung et al. **unsuitable for their intended purpose.**

Thus, even assuming arguendo, a proper motivation for combination, such combination could not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947*

F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

2. Claims 4 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., above, in view of Mizushima et al. (US 6,395,621).

Applicants reiterate the comments made above with respect to Leung et al.

The fact that Mizushima et al. disclose a method for forming raised source/drain structures from recrystallized silicon where a

gate oxide is disclosed may be tantalum oxide, does not further help Examiner in making out a *prima facie* case of obviousness. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 3, 11, 14, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., above.

Applicants reiterate the comments made above with respect to Leung et al.

"Finally, the prior art reference (or references when

combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

Conclusion

The cited references, neither individually nor in combination, produce Applicants disclosed and claimed invention, and therefore fail to make out a *prima facie* case of anticipation or obviousness with respect to Applicants independent, and therefore, dependent claims.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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